Epitaxial Graphene Nanoribbon Array Fabrication Using BCP-Assisted Nanolithography

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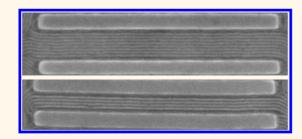
igh intrinsic carrier mobility, 1-3 high thermal conductivity, 4,5 and the one atom thick structure are some of the properties that make graphene an appealing material for high-speed electronics.^{6,7} However, the absence of a band gap in 2D graphene limits the on/off current ratio of graphene field-effect transistors (FET) to \sim 10 at room temperature, which is much lower than the requirement for digital electronics applications. Confining the carriers in graphene in the lateral dimension by fabricating graphene nanoribbons (GNRs) can induce a band gap whose magnitude depends on the width of the GNR, thus enabling higher on/off current ratios. The confinement induced band gap can be approximated by the formula⁸

$$\Delta E(W) = \frac{hv_0}{2W} = \frac{2.07 \text{ eV} \cdot \text{nm}}{W} \qquad (1)$$

where $v_0 = 10^{15}$ nm/s and W is expressed in nanometers.

Top-down approaches for fabricating GNR using graphene flakes and e-beam lithography^{9,10} lead to GNRs as narrow as 14 nm.9 The lowest GNR width attainable with this approach is limited by the resolution of e-beam lithography and increased line edge roughness (LER) at the resolution

Randomly dispersed GNRs narrower than 10 nm with atomically smooth edges have been formed by unzipping carbon nanotubes (CNTs)¹¹ or by ultrasonication of exfoliated graphite in an appropriate solution. 12 However, these methods suffer from the same fundamental problems that have limited up to now—the technological applicability of randomly deposited CNTs in the fabrication of large-scale electronic devices, that is, the lack of accurate and deterministic placement of CNTs with controlled diameter and **ABSTRACT**



A process for fabricating dense graphene nanoribbon arrays using self-assembled patterns of block copolymers on graphene grown epitaxially on SiC on the wafer scale has been developed. Etching masks comprising long and straight nanoribbon array structures with linewidths as narrow as 10 nm were fabricated, and the patterns were transferred to graphene. Our process combines both top-down and self-assembly steps to fabricate long graphene nanoribbon arrays with low defect counts. These are the narrowest nanoribbon arrays of epitaxial graphene on SiC fabricated to date.

KEYWORDS: epitaxial graphene · SiC · nanoribbon · nanolithography · block copolymer

chirality, as well as with high CNT area density. Thus, while these are very effective ways to explore experimentally the properties of GNRs, we still need to find ways to fabricate dense arrays of parallel GNRs with well-controlled dimensions, at a large scale, using processes that are easily implementable within the framework of a microelectronics fabrication facility. For the same reasons, we need to use graphene synthesized at wafer scale, which circumvents the limitations presented by graphene flakes. 13,14 Use of graphene grown epitaxially on the Si face of SiC is important because the azimuthal orientation of such graphene is constant over the whole wafer, ensuring control over the azimuthal orientation of the fabricated GNRs.¹³

The self-assembly properties of block copolymers (BCP) offer a fast and high-yield

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approach of making lithography masks for producing graphene nanostructures, such as graphene nanomeshes¹⁵ and nanoperforated graphene.¹⁶ These methods adopted BCP formulations that resulted in the formation of a cylindrical phase within a matrix and used them as etching masks to make nanosized holes in graphene, so that the graphene bridges between the holes had average lateral dimensions of several nanometers. The resulting carrier confinement led to the opening of a band gap and thus increased the on/off ratio of graphene nanomesh FETs; however, these graphene structures consisted of areas with variable widths and irregular, curved edges. The latter increase carrier scattering and are difficult to study and model.^{15,16} Here, we introduce a hybrid approach using a lamella-forming BCP to create straight GNR arrays bounded by pairs of parallel lines fabricated topdown by e-beam lithography (such lines can also be formed by photolithography) on graphene grown epitaxially on SiC wafers.

RESULTS AND DISCUSSION

Epitaxial graphene was grown on semi-insulating 6H(0001) SiC wafer surfaces by subtractive epitaxy in a multistep process that ended with an annealing step at 1550 °C in argon at a pressure of a few mTorr.^{17,18}

The repeat unit in diblock copolymers consists of two types of polymer blocks connected with each other by a covalent bond. These two polymer blocks phase-separate into periodic nanometer-scale domains under certain conditions. 19,20 The shape of the phase-separated domains can be spheres, cylinders, or lamellae, depending on the composition of the polymer and other parameters.²¹ We used the BCP polystyrene-*b*-poly(methylmethacrylate) (PS-*b*-PMMA) with molecular weight MW = 22k-22k g/mol, which under appropriate conditions phase-separates into alternating PS and PMMA lamellae having their long axis parallel to the substrate surface and each other and exhibiting a pitch of 25 nm. The PS-b-PMMA is dissolved in propylene glycol methyl ether acetate (PGMEA) at a concentration of 2 wt %. The two domains in this BCP exhibit different etching rates in reactive ion etching (RIE) processes using O₂ plasma. PMMA is etched faster than PS, and thus, after all the PMMA lamellae have been etched away, the remaining PS lamellae can be used as the etching mask for patterning graphene nanoribbons.

The lamellae need to stand perpendicular to the substrate surface and to be packed side by side with their long axis parallel to the substrate (Figure 1). Depending on the relative affinity of the surface to the PS and PMMA domains, the repeat direction of the lamellae can be either parallel or perpendicular to the substrate plane. In other words, a substrate surface with higher affinity for either PS or PMMA would force the BCP to form by stacking alternating layers of the

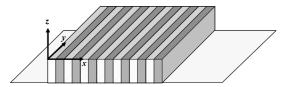


Figure 1. Alternating lamellae of the two components of a phase-separated BCP. Each of these lamellae has it long axis (y) parallel to the substrate and the longest dimension of its xz cross section, which in this scheme is along the z-axis, perpendicular to the substrate surface. Such lamellae are considered as standing perpendicular to the substrate surface, as opposed to ones that have the longest dimension of their xz cross section parallel to the substrate surface and are considered as lying parallel to the substrate.

two blocks, starting with the one having the highest affinity to the substrate. This can be avoided by using a neutralization layer below the BCP that has similar affinity for both of the BCP blocks, so that the PS and PMMA lamellae form perpendicular to the surface. The neutralization layer we used was the random copolymer poly(styrene-*r*-methylmethacrylate-*r*-glycidylmethacrylate) (P(S-r-MMA-r-GMA)) with 10 wt % thermal acid generator (TAG), dissolved in PGMEA at a concentration of 1 wt %. With the neutralization layer underneath, the BCP formed alternating PS and PMMA lamellae that stand normal to the substrate surface (Figure 1) and display a fingerprint pattern in top view, as shown in the top-down scanning electron microscopy (SEM) image of Figure 2a, where the bright lamellae are PS and the dark are PMMA. We find that the period of the pattern is about 25 nm (Figure 2b). There are two major methods to remove the PMMA domain of BCP selectively. One is the dry method of etching away the PMMA using an O₂ plasma RIE. Almost half of the PS thickness will remain after etching because the etching selectivity of PMMA/PS is about 2:1. Figure 2b shows a cross-section SEM of the phase-separated BCP layer that has undergone RIE using O₂ plasma for 43 s. Note that while the PS domain remains on the surface of the wafer, the PMMA domain has been removed, and the remaining PS lamellae have a width of 11-12 nm. A slightly longer etching time further reduces the width of the remaining PS lamellae to below 10 nm, as shown in Figure 2c. According to eg 1, a 10 nm wide GNR has a band gap of approximately 0.21 eV. The other PMMA etching method is a wet technique, which requires a UV exposure to create polymer chain scission in the PMMA domain followed by the removal of PMMA in acetic acid. The latter method is good for cylinderforming BCP but, when applied to lamellar formations, it results in the collapse of the BCP lamellae. This is due to capillary forces that cause the collapse of the lamellae during the drying of the sample, after it is soaked in liquids.²² Figure 2d shows the collapsed lamellae after using the wet method. Therefore, in this work, we use O2 RIE to selectively remove the PMMA lamellae and form the standing-up PS lamellae structure.

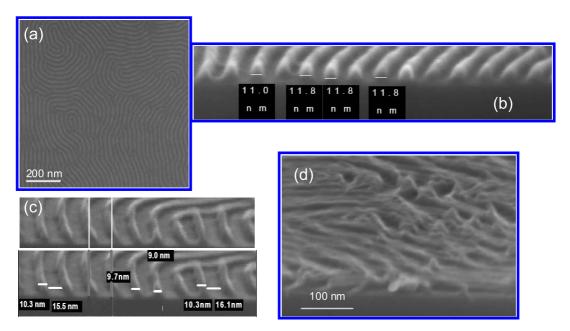


Figure 2. (a) Top-view SEM of the lamellae-forming BCP (PS-b-PMMA 22k-22k) on the surface of graphene coated with NFC and the neutralization layer. The scale bar is 200 nm. (b) Cross-section SEM image of the film depicted in (a) after etching the PMMA using O_2 RIE for 43 s. The PS lamellae have width between 11 and 12 nm. (c) The width of the PS lamellae is reduced further by slightly longer RIE (few seconds more) of the BCP structure without, however, creating any discontinuities in the PS structure. Lamella widths of 10 nm or below are attainable by this method. Both panels are the same, except for the annotations on the bottom panel. (d) PS lamellae collapse during wet etching, thus RIE etching is the appropriate way to remove the PMMA lamellae selectively. The scale bar is 100 nm.

To make straight and parallel BCP lamella arrays, we fabricated a larger scale pattern of parallel straight line segments on the surface, so that the PS and PMMA lamellae extend along a preferential orientation relative to the latter pattern (usually parallel to the straight line segments), a process called graphoepitaxy. We utilized the affinity of one of the BCP components to a specific material whose pattern was used to induce graphoepitaxy to the BCP. Hydrogen silsesquioxane (HSQ) was chosen since it is preferentially wetted by PMMA. PMMA will contact HSQ and guide the formation of the BCP pattern along the HSQ lines.^{23,24} The HSQ lines were fabricated by electron beam lithography (EBL), with lengths of 2 μ m and line spacings of 170, 270, and 370 nm. We note that, for the dimensions used, standard photolithography could have also been employed. Figure 3a,b shows top-view SEM images, exhibiting straight, aligned BCP lamellae formed between the HSQ lines with spacings of 270 and 170 nm, respectively. However, curved lamellae formed between the HSQ lines with 370 nm spacing (Figure 3c). From these results, it seems that there is a specific range for the HSQ spacing that promotes formation of perfectly straight lamellae, and this range is most probably dependent on the molecular weight of the BCP components.

Another important aspect of prepatterning the substrate arises from the hydrophobic nature of graphene. Due to the low surface energy of graphene, a wetting layer is needed between graphene and the first copolymer layer, so that the latter can be coated uniformly on

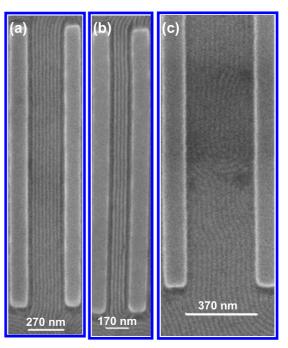


Figure 3. Lamellae form well between HSQ lines with (a) 270 nm and (b) 170 nm spacing, but they become curved when the spacing is bigger, e.g., 370 nm. The scale bar in each image is the same as the spacing size.

graphene. In this work, we used a polyhydroxystyrene derivative (commercial name NFC) as the wetting layer²⁵ to help the subsequent coating with the neutralization layer and BCP. The presence of this polymer directly on top of graphene has been shown to prevent the carrier mobility degradation observed previously with other

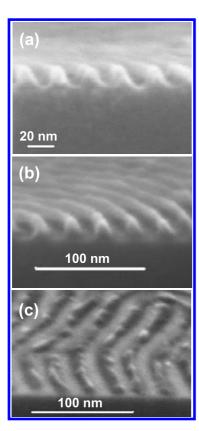


Figure 4. (a) 30 s RIE: etching reaches the substrate. (b) 43 s RIE: both the height and width of the PS lamellae decreased. (c) 51 s RIE: defects appear on the PS lamellae.

dielectric stacks, thus allowing for high field-effect mobilities to be retained in top-gated device operation.²⁵ Thus, it is advantageous to leave this layer on the graphene after the GNR patterning, as it acts as a buffer layer that reduces the performance, diminishing interactions of graphene with most of the gate dielectrics currently used in top-gated graphene device channels.

Subsequently, and due to the small initial thickness of the BCP (about 32 nm), we optimized the O_2 plasma RIE parameters required to completely etch through the PMMA domain, the neutralization layer (P(S-r-MMA-r-GMA)/TAG), the NFC, and the two layers of graphene, without creating any defects in the remaining PS etch mask.

For the RIE time optimization, all other parameters were kept constant. The RF power used was 50 W, the O_2 flow rate was 20 sccm, and the pressure was 30 mTorr. Within 30 s of RIE, the PMMA domain is completely removed, as shown in Figure 4a, and the height of the PS lamellae is about 22 nm. After 43 s, the lamellae in the PS domain are still defect-free, as shown in Figure 4b, and have a height of 14–15 nm. After a total RIE time of 51 s, many discontinuities appear on the PS lamellae, as shown in Figure 4c. If we limit the RIE duration time to about 43 s, the PS mask is thick enough to allow the removal of the two layers of graphene between the PS lamellae, while the

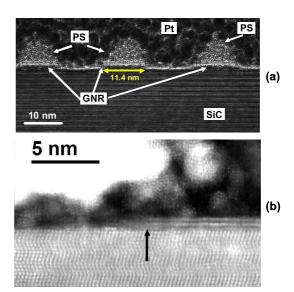


Figure 5. (a) TEM cross section taken from the sample that also appears on Figure 2b. We clearly observe that the graphene has been preserved below the PS lamellae, while it has been etched away completely between the PS lamellae, where the PMMA lamellae existed before RIE. The width of the resulting GNRs is again between 11 and 12 nm (the yellow arrow below the middle GNR is 11.4 nm long), that is, the same as the width of the PS lamellae measured on the SEM cross section of Figure 2b. (b) Filtered atomic resolution image recorded with a probe-corrected FEI Titan STEM operated at 200 kV. It shows clearly a graphene bilayer under the PS lamella on a flat SiC surface. The graphene bilayer is terminated abruptly at the region indicated by the black arrow. Outside the PS mask, Pt is in intimate contact with the SiC surface, and no graphene has been left after RIE.

graphene nanoribbons that are formed below the PS are protected.

To demonstrate that we have indeed fabricated GNRs with widths similar to the PS lamella width determined by cross-section SEM, we used transmission electron microscopy (TEM) to examine cross sections of samples like the one depicted in Figure 2b, which were produced in a dual-beam focused ion beam (FIB) tool. These cross sections were as close to perpendicular to the PS lamellae as possible. Imaging was performed at 300 kV using low dose methods to locate and align the sample. TEM images were recorded near Scherzer defocus. Figure 5a shows a TEM cross section of the sample that also appears on Figure 2b (43 s O₂ plasma RIE). We clearly observe that the graphene has been preserved below the PS lamellae, while it has been etched away completely between the PS lamellae, where the PMMA lamellae existed before RIE. The width of the resulting GNRs is again between 11 and 12 nm (the arrow below the middle GNR is 11.4 nm), that is, the same as the width of the PS lamellae determined by cross-section SEM. From this, we can conclude that the lamella width of the PS mask determines the width of the GNR. The height of the remaining NFC/neutralization layer/PS mask does not exceed 7 nm. The very faint—compared to the GNRsstructure appearing in some areas outside the PS lamellae is not due to remnants of graphene but due to projection effects caused by the finite thickness of the sample cross section used and the fact that the lamellae in this sample were not straight lines but exhibited the pattern depicted in Figure 2a. This interpretation is corroborated by the scanning transmission electron microscopy (STEM) results described below. We obtained high-resolution dark-field images using an aberration-corrected STEM operated at 200 kV. This allowed us to observe directly the graphene layers, without the fringing effects and the dependence on the defocus condition that is present in phase-contrast TEM mode. Figure 5b shows a filtered

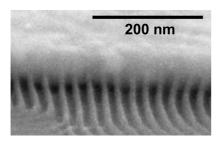


Figure 6. PS lamellae form perpendicular to the Au edge (light gray region on the top half of the image) in the vicinity of the metal, a direction that coincides with the direction of the HSQ guiding pattern in our FET fabrication scheme.

atomic resolution STEM image recorded in this way. It shows clearly a graphene bilayer (as expected from the graphene growth conditions) under a PS lamella on a flat SiC surface. The graphene bilayer is terminated abruptly at the region indicated by the black arrow. Outside the PS mask, the Pt grains are in intimate contact with the SiC surface, and no graphene is left after RIE.

After the O₂ plasma treatment, the PS domain could not be removed by exposure to hot acetone and other common solvents like toluene. This may be attributed to the oxidation and hardening of the PS in the oxygen plasma. Therefore, when fabricating GNR field-effect transistors (FET), the source/drain contacts to graphene should be formed prior to coating it with the polymers used in this patterning process. Additionally, instead of trying harsh chemicals or methods to remove the PS lamellae from the top of the GNRs, we believe that PS can become an integral part of the dielectric stack of top-gated GNR devices, especially after considering the positive effect that the polyhydroxystyrene layer underlying the PS has in preventing the mobility degradation of graphene, as discussed above and in ref 25.

The metal edge does not affect the desired orientation of the lamellae if we also coat the metal with the neutralization layer.²⁶ The lamellae are perpendicular

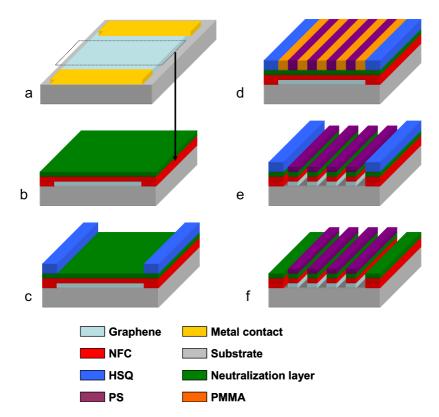


Figure 7. Fabrication flow of using BCP to make graphene nanoribbon devices. (a) Isolate graphene channel from surrounding graphene, and contact graphene by metal leads. (b) Coat the sample with NFC and neutralization layer. (c) Write HSQ lines by electron beam lithography and develop in TMAH. (d) Coat the sample with BCP, and anneal at 240 $^{\circ}$ C for 2 min, the PS and PMMA domains form. (e) Etch PMMA and the other polymers as well as the graphene with O_2 RIE. (f) Remove the HSQ pattern, immersing the sample in a HF acid solution.

to both the metal electrode side surface and the substrate surface, which is the desired orientation. HSQ is still required as the guiding pattern for graphoepitaxy because the neutralized metal sidewall can force the straight lamellae to extend over only a relatively short distance from the metal edge, approximately 100 nm, while curved lamellar domains appear at longer distances. Figure 6 shows the lamellae forming at the metal edge coated with the neutralization layer and their transition from straight to curved, approximately 100 nm from the metal edge.

The HSQ lines can be removed by soaking the sample in a HF solution. The acid reaches the HSQ through the slits formed in the BCP by the etching of the PMMA domains. The entire process design and fabrication flow is shown in Figure 7. We begin with a layer of epitaxial graphene grown on top of a SiC substrate. We then define an initial FET channel and isolate it from the surrounding graphene with lithography and oxygen RIE, followed by connecting the graphene channel with metal leads (e.g., Pd/Au with 30/30 nm thickness), shown in Figure 7a, using a lift-off process.^{6,17} The metal leads are not shown in the subsequent illustrations in order to depict more clearly the following process steps. We then spin coat NFC and bake it at 175 °C for 1 min, spin coat the neutralization layer (P(S-r-MMA-r-GMA)/TAG), and bake it at 200 °C for 30 min, spin coat some PGMEA until the film is dry, and then bake at 200 °C for 2 min, as shown in Figure 7b. In Figure 7c, the fabrication of the HSQ line pattern is shown. These lines have a length of 2 μ m, and the development is done in a solution of tetramethylammonium hydroxide (TMAH). Then we coat the sample with BCP and bake it at 240 °C for 2 min.

The PMMA and PS domains phase-separate, forming straight lamellae between the HSQ lines, as shown in Figure 3 (actual sample) and Figure 7d. O₂ plasma RIE is used to remove the PMMA domains and the other polymers underneath and to etch graphene (Figure 7e). Finally, the HSQ lines are removed by soaking the sample in a HF solution (Figure 7f).

CONCLUSION

In conclusion, we have developed a process enabling us to fabricate arrays of epitaxial graphene nanoribbons with GNR width as low as 10 nm. This hybrid process comprises two main complementary steps: a top-down e-beam lithography step (which could also be performed by standard photolithography using an appropriate photolithographic mask), and a bottom-up self-assembly step involving a block copolymer template. Such GNR widths are very difficult to achieve using conventional top-down lithography alone, either photolithography or e-beam lithography. These are the narrowest epitaxial graphene nanoribbons on SiC fabricated to date. A number of materials appropriate to the present task and a series of process steps that complement the two main steps described above had to be selected, developed, and optimized. They include BCP molecular weight and thickness, the neutralization layer composition, the HSQ graphoepitaxy mask direction, and line spacing, and the RIE process chemistry and parameters needed to achieve the narrowest, continuous GNRs with smooth edges. These processes are readily available for future fabrication and testing of FETs and other devices comprising arrays of the narrowest nanoribbons of epitaxial graphene demonstrated to date.

METHODS

Epitaxial graphene was grown on semi-insulating 6H(0001) SiC wafer surfaces within a cylindrical, induction-heated graphite susceptor installed in a UHV chamber. We used a multistep process comprising two surface preparation steps, annealing at 810 $^{\circ}\text{C}$ for 10 min and 1140 $^{\circ}\text{C}$ for 7 min (both under flow of 20% disilane in He), and a graphenization step, heating at 1550 $^{\circ}\text{C}$ for 10 min under Ar flow at a chamber pressure of 3.5 mTorr. 17,18

Top-down and cross-section SEM were obtained at a few kilovolts using a field emission SEM instrument.

TEM and STEM cross sections were produced in a FEI Helios dual-beam FIB using SEM imaging at 2 kV, Pt deposition induced by a 2 kV e-beam to mask the area of interest without any appreciable damage, cross section cutting with standard Ga FIB, and finally, a low-energy Ga ion beam clean. The cross sections were lifted out onto an amorphous carbon-coated Cu grid ex situ. Imaging was performed on a JEOL 3000F microscope at 300 kV using low dose methods to locate and align the sample. TEM images were recorded near Scherzer defocus. High-resolution dark-field STEM images were obtained using an aberration-corrected FEI Titan STEM operated at 200 kV.

Conflict of Interest: The authors declare no competing financial interest.

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Note added in Proof: During the review process, a recent publication came to the attention of the authors, which reported GNRs with width ~ 10 nm using e-beam lithography. Reference: Hwang, W. S.; Tahy, K.; Nyakiti, L. O.; Wheeler, V. D.; Myers-Ward, R. L.; Eddy, Jr., C. R.; Gaskill, D. K.; Xing, H. (G.); Seabaugh, A.; Jena D. J. Vac. Sci. Technol. B 2012, 30, 03D104.

REFERENCES AND NOTES

- Morozov, S. V.; Novoselov, K. S.; Katsnelson, M. I.; Schedin, F.; Elias, D. C.; Jaszczak, J. A.; Geim, A. K. Giant Intrinsic Carrier Mobilities in Graphene and Its Bilayer. *Phys. Rev. Lett.* 2008, 100, 016602.
- Bolotin, K. I.; Sikes, K. J.; Jiang, Z.; Fudenberg, G.; Hone, J.; Kim, P.; Stormer, H. L. Ultrahigh Electron Mobility in Suspended Graphene. Solid State Commun. 2008, 146, 351–355.
- Du, X.; Skachko, I.; Barker, A.; Andrei, E. Y. Approaching Ballistic Transport in Suspended Graphene. *Nat. Nano-technol.* 2008, 3, 491–495.

- Balandin, A. A.; Ghosh, S.; Bao, W.; Calizo, I.; Teweldebrhan, D.; Miao, F.; Lau, C. N. Superior Thermal Conductivity of Single-Layer Graphene. *Nano Lett.* 2008, 8, 902–907.
- Balandin, A. A. Thermal Properties of Graphene and Nanostructured Carbon Materials. *Nat. Mater.* 2011, 10, 569–581.
- Lin, Y.-M.; Dimitrakopoulos, C.; Jenkins, K. A.; Farmer, D. B.; Chiu, H. Y.; Grill, A.; Avouris, Ph. 100-GHz Transistors from Wafer-Scale Epitaxial Graphene. Science 2010, 327, 662.
- 7. Lin, Y.-M.; Valdes-Garcia, A.; Han, S.-J.; Farmer, D. B.; Meric, I.; Sun, Y.; Wu, Y.; Dimitrakopoulos, C.; Grill, A.; Avouris, Ph.; et al. Wafer-Scale Graphene Integrated Circuit. Science **2011**, *332*, 1294–1297.
- 8. Berger, C.; Song, Z. M.; Li, X. B.; Wu, X. S.; Brown, N.; Naud, C.; Mayo, D.; Li, T. B.; Hass, J.; Marchenkov, A. N.; et al. Electronic Confinement and Coherence in Patterned Epitaxial Graphene. Science 2006, 312, 1191–1196.
- Han, M. Y.; Özyilmaz, B.; Zhang, Y.; Kim, P. Energy Band-Gap Engineering of Graphene Nanoribbons. *Phys. Rev. Lett.* 2007, 98, 206805.
- Chen, Z.; Lin, Y.-M.; Rooks, M. J.; Avouris, Ph. Graphene Nano-ribbon Electronics. *Physica E* 2007, 40, 228–232.
- Kosynkin, D. V.; Higginbotham, A. L.; Sinitskii, A.; Lomeda, J. R.; Dimiev, A.; Price, B. K.; Tour, J. M. Longitudinal Unzipping of Carbon Nanotubes To Form Graphene Nanoribbons. *Nature* 2009, 458, 872–877.
- Li, X.; Wang, X.; Zhang, L.; Lee, S.; Dai, H. Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors. Science 2008, 319, 1229–1232.
- 13. Avouris, Ph.; Dimitrakopoulos, C. Graphene: Synthesis and Applications. *Mater. Today* **2012**, *10*, 86–97.
- Dimitrakopoulos, C.; Grill, A.; McArdle, T. J.; Lin, Y. M.; Liu, Z.; Pfeiffer, D.; Wisnieff, R.; Avouris, Ph. Optimization of Wafer-Scale Epitaxial Graphene on SiC for RF Applications. GraphITA Workshop 2011, Gran Sasso National Laboratories, Assergi-L'Aquila, Italy. Invited extended abstract L05 (pp.1-4), URL: http://graphita.bo.imm.cnr.it/program. html#SessionD
- 15. Bai, J.; Zhong, X.; Jiang, S.; Huang, Y.; Duan, X. Graphene Nanomesh. *Nat. Nanotechnol.* **2010**, *5*, 190–194.
- Kim, M.; Safron, N. S.; Han, E.; Arnold, M. S.; Gopalan, P. Fabrication and Characterization of Large-Area, Semiconducting Nanoperforated Graphene Materials. *Nano Lett.* 2010, 10, 1125–1131.
- Dimitrakopoulos, C.; Lin, Y.-M.; Grill, A.; Farmer, D. B.; Freitag, M.; Sun, Y.; Han, S.-J.; Chen, Z.; Jenkins, K. A.; Zhu, Y.; et al. Wafer-Scale Epitaxial Graphene Growth on the Si-Face of Hexagonal SiC (0001) for High Frequency Transistors. J. Vac. Sci. Technol., B 2010, 28, 985–992.
- Dimitrakopoulos, C.; Grill, A.; McArdle, T. J.; Liu, Z.; Wisnieff, R.; Antoniadis, D. A. Effect of SiC Wafer Miscut Angle on the Morphology and Hall Mobility of Epitaxially Grown Graphene. Appl. Phys. Lett. 2011, 98, 222105.
- Stoykovich, M. P.; Nealey, P. F. Block Copolymers and Conventional Lithography. *Mater. Today* 2006, 9, 20–29.
- Bang, J.; Jeong, U.; Ryu, D. Y.; Russell, T. P.; Hawker, C. J. Block Copolymer Nanolithography: Translation of Molecular Level Control to Nanoscale Patterns. Adv. Mater. 2009, 21, 4769–4792.
- Bates, F. S.; Fredrickson, G. H. Block Copolymer Thermodynamics Theory and Experiment. *Annu. Rev. Phys. Chem.* 1990, 41, 525–557.
- Ting, Y. H.; Park, S. M.; Liu, C. C.; Liu, X.; Himpsel, F. J.; Nealey, P. F.; Wendt, A. E. Plasma Etch Removal of Poly(methyl methacrylate) in Block Copolymer Lithography. J. Vac. Sci. Technol., B 2008, 26, 1684–1689.
- Yamaguchi, T.; Yamaguchi, H. Two-Dimensional Patterning of Flexible Designs with High Half-Pitch Resolution by Using Block Copolymer Lithography. Adv. Mater. 2008, 20, 1684–1689.
- Cheng, J. Y.; Rettner, C. T.; Sanders, D. P.; Kim, H.-C.; Hinsberg, W. D. Dense Self-Assembly on Sparse Chemical Patterns: Rectifying and Multiplying Lithographic Patterns Using Block Copolymers. Adv. Mater. 2008, 20, 3155–3158.

- Farmer, D. B.; Chiu, H.-Y.; Lin, Y. M.; Jenkins, K. A.; Xia, F.; Avouris, Ph. Utilization of a Buffered Dielectric To Achieve High Field-Effect Carrier Mobility in Graphene Transistors. Nano Lett. 2009, 9, 4474–4478.
- Park, S. M.; Rettner, C. T.; Pitera, J. W.; Kim, H. C. Directed Self-Assembly of Lamellar Microdomains of Block Copolymers Using Topographic Guiding Patterns. *Macromolecules* 2009, 42, 5895–5899.