1/f Noise Characteristics of MoS_2 Thin-Film Transistors: Comparison of Single and Multilayer Structures

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***Abstract*— We report on the transport and low-frequency noise measurements of MoS_2 thin-film transistors (TFTs) with thin (2–3 atomic layers) and thick (15–18 atomic layers) channels. The back-gated transistors made with the relatively thick MoS_2 channels have advantages of the higher electron mobility and lower noise level. The normalized noise spectral density of the low-frequency 1/f noise in thick MoS_2 transistors is of the same level as that in graphene. The MoS_2 transistors with the atomically thin channels have substantially higher noise levels. It was established that, unlike in graphene devices, the noise characteristics of MoS_2 transistors with thick channels (15–18 atomic planes) could be described by the McWhorter model. Our results indicate that the channel thickness optimization is crucial for practical applications of MoS_2 TFTs.**

***Index Terms*— MoS_2 thin-film transistor, noise, graphene.**

I. Introduction

ATOMICALLY thin two-dimensional (2D) materials – also referred to *as van der Waals* materials – are attracting attention for electronic, sensing and optical applications. So far, the most explored materials among them are graphene and one to several atomic layers MoS_2 [1]–[3]. While single-layer graphene is a zero band gap material, single-layer MoS_2 shows a direct band gap of $E_g \sim 1.9$ eV. As the number of layers increases, the band gap of MoS_2 decreases until it reaches its bulk value of 1.3 eV [2], [3]. With the exception of single-layer, thin films of MoS_2 of all other thicknesses, including bulk, are indirect band gap semiconductors. A relatively large band gap of atomic layers of MoS_2 is one of its main advantages over graphene, since it makes MoS_2 suitable for transistor applications. Unlike graphene devices, MoS_2 thin-film transistors (TFTs) demonstrate very high on-off ratios of up to 10^8 [1]–[3]. A relatively high mobility of up to a few hundreds of cm^2/Vs and high thermal conductivity of MoS_2 thin films [4] might make MoS_2 transistors competitive with α-Si and poly-Si TFTs.

An interesting feature of the 2D materials is the dependence of their properties on the number of the atomic layers. A proper selection of the thickness, i.e. number of atomic layers in MoS_2 films for specific device applications is one of the important issues in the development of the *van der Waals* materials technology. Compared to graphene and single layer MoS_2 devices, the multilayer MoS_2 TFTs have a higher stability, lesser sensitivity to the environment and higher electron mobility. In particular, as shown in [5], the electron mobility in MoS_2 films has maximum at thickness H=10 nm, which corresponds to approximately 15-16 layers of the material.

An important parameter for electronics and sensing applications of transistors is the level of the low-frequency electronic noise. In various types of sensors, the low frequency noise sets the sensitivity and selectivity limits. For high-frequency communication applications, the low-frequency noise is up converted to the phase noise, thus limiting the performance of every microwave and terahertz device. The studies of the low-frequency noise in MoS_2 transistors have already been reported in a number of publications [6]–[12]. The experimental results have been interpreted in the framework of either McWhorter number-of-carriers model [6]–[8], unified model incorporating carrier-number fluctuation and correlated mobility fluctuations, [9], [10] or expressed using the empirical Hooge formula [11]. In the majority of these publications, it was found that the normalized noise spectral density of the drain current, S_I/I^2, significantly decreased with the increasing gate voltage, V_g. One exception was the data presented in [12] showing a relatively weak gate voltage dependence with the maximum at a certain gate voltage (similar to such a dependence often found in graphene).

The decrease of the noise spectral density of the drain current with the gate voltage in MoS_2 TFT is similar to that for conventional Si metal-oxide-semiconductor field-effect

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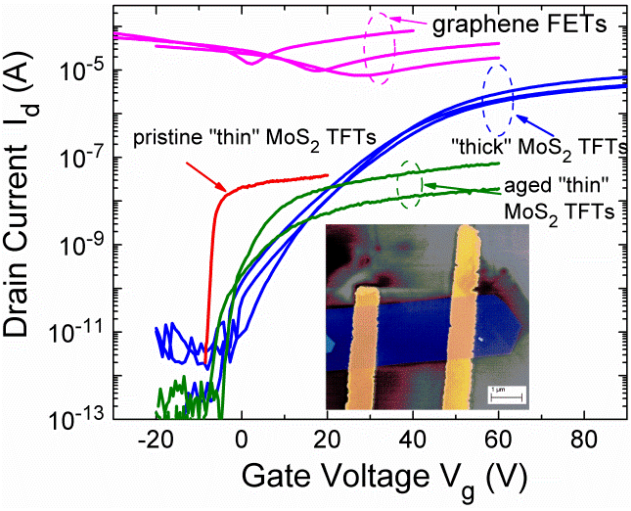

Fig. 1. Transfer current-voltage characteristics of graphene devices, MoS_2 TFT with "thick" channel (thickness H=15-18 atomic layers) and MoS_2 TFT with "thin" channel (H=2-3 atomic planes). The data for "thin" channel devices are shown for the pristine and aged devices. Inset shows scanning electron microscopy image of a typical MoS_2 TFT. The pseudo-colors are used for clarity: blue is MoS_2 channel while yellow is metal contacts.

transistors (MOSFETs). In conventional MOSFETs, in the majority of cases, the low-frequency noise complies with the McWhorter model [13], which predicts the decrease of S_I/I^2 as $1/(V_g\text{-}V_t)^2$, where V_t is the threshold voltage. This makes the noise properties of MoS_2 TFT qualitatively similar to those in MOSFETs and different from those in graphene devices. Typically, the noise in graphene transistors only weakly depends on the gate voltage [14], [15] being within the range $S_I/I^2 \times A = 10^{-8} - 10^{-7}\mu m^2/Hz$ (A is the channel area) [15]. In comparison, in Si MOSFETs noise changes by many orders of magnitude decreasing with the gate voltages as $S_I/I^2 \sim 1/(V_g\text{-}V_t)^2$, in accordance with the McWhorter model.

In the present work, we report on the low-frequency noise in "thin" (2-3 layers) and "thick" (15-18 layers) back-gated MoS_2 TFTs. The focus of this study is the comparison of the noise levels in these two types of MoS_2 TFTs with noise data published for back-gated graphene devices. Thin films of MoS_2were prepared by a standard exfoliation method and placed on Si/SiO_2 substrates. Details of material preparation can be found in [17] and references therein. The thickness and quality of thin films were determined with the atomic force microscopy (AFM) and micro-Raman spectroscopy. The drain and source Ti/Au (10-nm/100-nm) contacts were fabricated using the electron-beam lithography (LEO SUPRA 55) for patterning of the source and drain electrodes and the electron-beam evaporation (Temescal BJD-1800) for metal deposition. The heavily doped Si/SiO_2 wafer served as a back gate. The channel length, L, and width, W, varied within the range from 1.3 μm to 6 μm. The inset in Fig. 1 shows a schematic and scanning electron microscopy (SEM) image of a typical fabricated MoS_2 TFT.

Figure 1 presents the transfer current-voltage characteristics of MoS_2 TFTs with different channel thicknesses. The lateral dimensions of all examined devises are similar. The characteristics for graphene devices are also shown for the comparison. Some specific advantages and disadvantages of these three systems are already seen from these current-voltage characteristics. While graphene device are characterized by a small on-off ratio, I_{on}/I_{off}, the MoS_2 TFTs demonstrate $I_{on}/I_{off} > 10^5$. Graphene devices have substantially higher current levels than the "thin" (2-3 layers) MoS_2 TFTs owing to a much higher carriers mobility in graphene. The drain current in the "thick" (15-18 layers) MoS_2 TFTs is higher than that in "thin" MoS2 TFTs and approaches the typical values for graphene devices. The subthreshold voltage slope in the "thick" MoS_2 TFTs is smaller than that in the "thin" MoS_2 TFTs, i.e. a higher gate voltage swing is required to switch the "thick" MoS_2 TFTs.

Plotting the drain-to-source resistance, R_{ds}, vs. $1/(V_g\text{-}V_t)$, and extrapolating this dependence to zero yielded the estimate for the total contact resistance, which is negligible for the "thick" MoS_2 devices compared to the channel resistance.

The field-effect mobility, μ_{FE}, in TFTs was calculated as

$$\mu_{FE} = \frac{g_m L}{C_{ox} V_d W}. \quad (1)$$

Here, g_m is the transconductance, $C_{OX} = \varepsilon_o \varepsilon_r / d = 1.15 \times 10^{-4}$ (F/m^2) is the oxide capacitance, ε_o is the dielectric permittivity of free space, ε_r is the dielectric constant, and d is the oxide thickness. We used $\varepsilon_r = 3.9$ and $d = 300$ nm for the SiO_2 layer. We found the field-effect mobility within the range $\mu_{FE} = 0.5 - 8$ cm^2/Vs for "thin" MoS_2 devices (thickness H = 2-3 atomic layers) and $\mu_{FE} = 20 - 80$ cm^2/Vs for "thick" MoS_2 devices (H = 15-18 atomic layers). The fact that the mobility in "thick" MoS_2 TFTs is on the order of magnitude higher than that in "thin" devices is in agreement with the results reported in Ref. [5]. Overall, the mobility values in our "thin" and "thick" MoS_2 TFTs are typical for such back-gated devices and in agreement with the previously reported values [5].

The low-frequency noise was measured under ambient conditions at room temperature (RT) in the linear regime at the drain voltage $V_d = 50 - 100$ mV. The low-frequency noise was of the $1/f^{\alpha}$ type without any generation-recombination bulges. The extracted exponent is $\alpha = 0.75 - 1.25$. Figure 2 compares the gate-voltage dependence of 1/f noise spectral density normalized to the device area for four types of devices: "thin" MoS_2 TFTs (H=2-3 atomic layers), "thick" MoS_2 TFTs (H=15-18 atomic layers), single layer graphene field-effect transistors (FETs), and thick layer graphene. As seen, "thick" MoS_2 TFTs have smaller noise levels, comparable to that in graphene devices. While at small gate voltage, the noise levels in "thin" and "thick" MoS_2 films are comparable, at $(V_g\text{-}V_t) > 10$ V, the noise level in "thick" MoS_2 films is much smaller. We attribute the noise increase in "thin" MoS_2 films with the gate voltage to the contribution of the contact noise and effects of the fast aging of these devices. The technology of contacts fabrication to MoS_2 is still under development and contact resistance to 1-3 layer material is usually not negligible [18]. As a result, contribution of contacts to noise can be quite large and this contribution increases

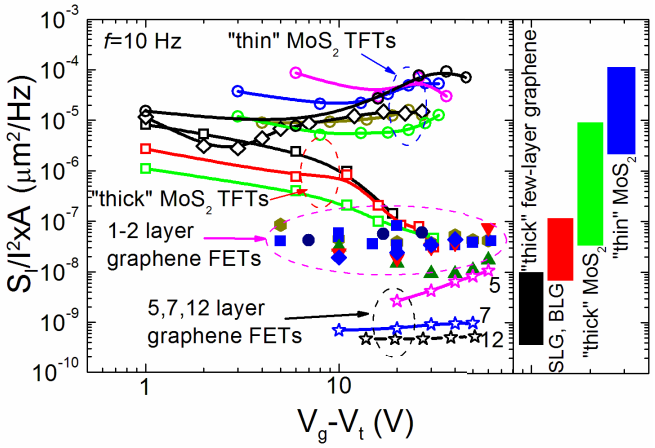

Fig. 2. Right panel: Comparison of the noise spectral density versus gate voltage dependences for MoS_2 TFTs with "thick" channel (H = 15-18 atomic layers), MoS_2 TFTs with "thin" channel (H = 2-3 atomic planes), single and bi-layer graphene devices (SLG, BLG), and multi-layer graphene devices. The data for graphene devices are taken from Ref. [15], [16]. Black diamond symbols show the data for as fabricated "thin" MoS_2 transistor. Other symbols for "thin" MoS_2 transistor represent noise data for several devices with different stages of aging ranging from 2 days to several weeks. The "thick" channel transistors demonstrated good stability in current voltage characteristics and noise behavior over at least one month. The data for three TFTs are shown. Left panel: noise ranges for the studied devices.

with the channel resistance decrease, i.e. with the gate voltage increase (see [6], for example.). Transistors with thicker MoS_2 channel usually suffer less from high contact resistance. This is probably due to the smaller channel sheet resistance and higher contact transfer length [19]. Faster aging of "thin" MoS_2 films is probably due to its ultimate surface to volume ratio.

The McWhorter model allows estimating the trap density responsible for the low-frequency noise [13] from the drain current fluctuation density, S_I/I^2, or from the equivalent voltage fluctuations, $S_V = S_I/g_m^2$, where g_m is the transconductance. In the latter case, the trap density can be estimated as

$$N_t = S_v \frac{\gamma f W L C_{ox}^2}{kTq^2}, \qquad (2)$$

where k is the Boltzmann constant, T is absolute temperature, γ is the tunneling parameter conventionally assumed to be $\gamma = 10^8$ cm^{-1}, and N_t is the trap density. The advantage of using this approach in comparison with the trap density estimation from the drain current fluctuations is that it is independent of the threshold voltage, V_t, which can have high uncertainty is some cases. Our estimate for the TFTs with the "thick" MoS_2 channel yields $N_t \approx 10^{18}$ cm^{-3}eV^{-1} (for the smallest noise device with the characteristics shown in Fig.2). This value is about one order-of-magnitude smaller than that for as fabricated MoS_2 TFTs with H = 3 atomic planes described in Ref. [6]. However the absolute value of the trap density extracted is still higher than that for Si MOSFETs with high quality SiO_2. This is probably due to the specific technology of the MoS_2 exfoliation and deposition. On the other hand extracted trap density is within the limit found for conventional FETs with high-k dielectric [20].

The interface trap density for MoS_2 TFTs with the channels of a similar thickness was found to be $N_{it} = (5.5 - 7.2) \times 10^{10}$ cm^{-2}eV^{-1} [8]. An estimate of the interface trap density depends on the estimation of the characteristic tunneling depth in SiO_2. Using the same approach as in [8], we obtain $N_{it} \approx 10^{10}$ cm^{-2}eV^{-1}, which is only slightly smaller than the value in [8].

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