Transistor-Less Logic Circuits Implemented With 2-D Charge Density Wave Devices

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***Abstract*— We propose logic gates and circuits implemented with 2-D charge density wave (CDW) devices, which operate at room temperature. The 1T-TaS_2 charge density wave devices exhibit a voltage triggered phase transition between the nearly commensurate and incommensurate CDW states, which is accompanied by an abrupt change of the resistance and hysteresis. The unique output characteristics of such devices allow for building logic gates and circuits without any transistors. Using the experimentally measured current–voltage characteristics, we model and numerically simulate the performance of the inverter and the OR logic gates consisting of CDW devices and regular resistors. Owing to the radiation-hard nature of the CDW devices and absence of transistors, the proposed circuits can be utilized in various harsh environments on earth or outer space.**

***Index Terms*— Logic gates, charge density wave devices, radiation hardness.**

I. Introduction

RADIATION induced damage is one of the most important and challenging failure phenomena in modern electronics [1]. The problem is particularly acute for radiation - harsh environment of the outer space [2]. It is known that the performance of the metal-oxide-semiconductor (MOS) devices may degrade significantly due to X-ray or proton irradiation [3]. Electron–hole pairs generated in the oxide during the total-ionizing-dose (TID) irradiation can accumulate in the oxide layers and at the interfaces in the field effect transistor (FET) structures [4]. Downscaling of the modern FETs has drastically reduced the on-chip capacitances, leaving the logic in the recent generation hardware vulnerable to radiation-induced errors [5]. These facts explain an urgent need in the radiation-hardened electronics, able to overcome the physical limits of the MOS transistor technology. A radical solution to the problem would be a development of the circuits based on materials, which are less susceptible to radiation damage, and logic gates that do not involve transistors.

We have recently demonstrated that the charge density wave phase transitions in quasi-two-dimensional (2D) 1T-TaS_2 can be used to build voltage controlled oscillators (VCO) operating at room temperature (RT) [6]. Since CDW materials are metals or semimetals, with very high concentrations of electrons, they can be inherently more radiation hard than semiconductors. The radiation hardness of 1T-TaS_2 VCOs against X-rays has been proven directly experimentally [7].

Here we show that two-terminal CDW devices can be used to construct logic gates and circuits without any transistors. Specifically, we use 1T-TaS_2 films, which reveal a transition from the nearly commensurate CDW state (NC-CDW) to incommensurate CDW state (IC-CDW) at the temperature of 350 K. This transition can be triggered by a small voltage bias at lower temperatures [6]. The transition manifests itself as an abrupt change in the resistivity of the channel accompanied by a hysteresis. These characteristics are sufficient to construct the inverter and the OR logic gates, and perform information processing using circuits without transistors, in the radiation-hard environment.

II. CDW Devices as Logic Building Blocks

To demonstrate a feasibility of the approach, we fabricated a set of CDW devices using the shadow mask method [8]. The device consists of 1T-TaS_2 channel on a standard Si substrate with two metal contacts [6], [7]. The fabricated structures had several metal contacts, which each pair acting as a separate device. A typical threshold switching I-V characteristics of such 1T-TaS_2 device at RT are shown in Figure 1. The device is in the high resistive state R_H at zero bias voltage. The resistance drops significantly to R_L as the bias voltage exceeds the threshold value V_{HL}. The resistance returns to the initial high value R_H as the voltage is scanned back below the threshold value V_{LH}. The carrier concentrations in the both CDW states are very high: 10^{21} cm^{-3} and 10^{22} cm^{-3} for the high resistive NC-CDW and low resistive IC-CDW phases, respectively [6], [7], [9]. The experimental I-V characteristics were parametrized and used as inputs in the modeling experiments, which simulate the operation of the transistor-less logic gates implemented with 1T-TaS_2 CDW devices.

III. CDW Based Logic Gates

The schematic of the proposed CDW-based inverter is shown in Figure 2(a). It comprises two CDW devices and one regular resistor. The CDW devices are connected in series and biased by V_{DD}. The input and the output ports

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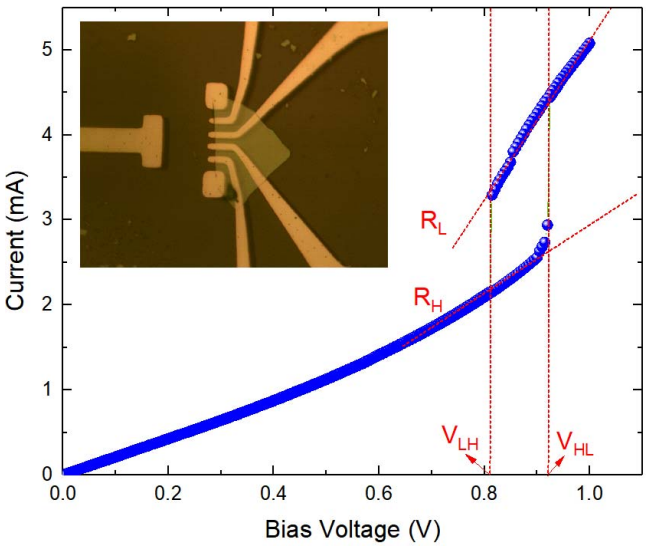

Fig. 1. Experimental *I-V* characteristics of a 1T-TaS_2 CDW device showing distinctive threshold switching at RT. The dashed line depicts the transitions between the NC-CDW and IC-CDW states. Inset is an optical microscopy image of a representative 1T-TaS_2 device.

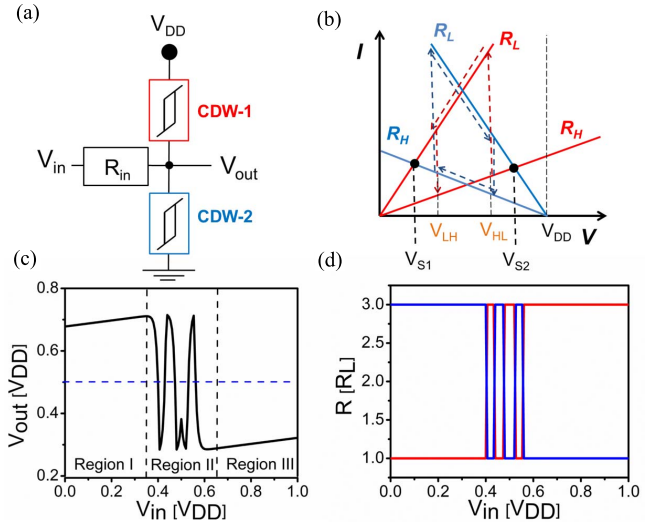

Fig. 2. (a) Schematic of the inverter gate consisting of two CDW devices and one regular resistor. (b) Phase space of the circuit comprising two CDW devices. (c) Results of numerical modeling showing the output voltage V_{out} as a function of V_{in}. (d) The change in the CDW resistances R_1 and R_2 as a function of V_{in}.

are connected in series through the center point between the CDW devices. The couple of CDW devices connected is series forms a complementary pair [10]. With a proper choice of the device parameters, R_H, R_L, V_{HL}, V_{LH}, and the bias voltage, V_{DD}, such a pair can be put in a self-sustaining oscillation regime, where one of the CDW devices is in the high resistance state while the other one is in the low resistance state. The conditions leading to the self-sustaining oscillations in the circuit comprising two CDW devices are illustrated in Figure 2(b). There are two stable points depicted by the black dots, which correspond to the two stable states of the system, *i.e.*, $V_{S1} = V_{DD} \cdot \frac{R_L}{[R_L+R_H]}$ and $V_{S2} = V_{DD} \cdot R_H/[R_L + R_H]$. However, the system cannot reach any of the stable states due to the phase transitions happening at $V_{LH} = V_{S1} + \Delta V$ and $V_{HL} = V_{S2} - \Delta V$, where ΔV is the voltage offset, discussed later in the text. Thus, the system of two CDW devices show permanent oscillations, which may continue for infinitely long time till the change of the bias voltage V_{DD}. We utilize the input voltage V_{in} to move the system out of the oscillatory regime towards the one of the stable states.

In Figure 2(c), we present the results of numerical modeling showing the change of the output voltage V_{out} as a function of V_{in}. In the model, we adopted the computational approach reported in [11]. The circuit dynamics can be described by the following set of piecewise linear differential equations

$$C\left(\frac{dV_{out}}{dt}\right) = \frac{(V_{DD} - V_{out})}{R_1} - \frac{V_{out}}{R_2} + \frac{V_{in}}{R}, \qquad (1)$$

where C is the lumped capacitance of both devices together with the parasitic capacitances, R_1 and R_2 are the resistances of the top and the bottom CDWs shown in Figure 1(a), and R is the input resistance. The CDW resistances R_1 and R_2 may be either R_L or R_H depending the path on the phase space as shown in Figure 2(b). Without the loss of generality, we take $R_L = 1\Omega$, $V_{DD} = 3.0\ V$, and normalize all other parameters to R_L and V_{DD} as follows: $R_H = 3R_L$, $R = 7R_L$, $\Delta V = 0.1V_{DD}$. There are three regions in the plot in Figure 2(c), which correspond to the different states ofthe circuit. Region I: $0 < V_{in} \leq 0.35V_{DD}$ corresponds to the high output voltage $V_{out} > 0.6\ V_{DD}$, which increases with increase of V_{in}. Region II: $0.35\ V_{DD} < V_{in} < 0.65V_{DD}$, corresponds to the oscillation regime, where V_{out} is within the range from 0.3 V_{DD} to 0.7 V_{DD}. Region III: $0.65\ V_{DD} < V_{in} < V_{DD}$, has the low output voltage, $V_{out} < 0.35V_{DD}$,, which increases with increase of V_{in}. In Figure 2(d), we depicted the change of the CDW resistances R_1 and R_2 as the function of V_{in}: $R_1 = R_H$ and $R_2 = R_L$ for region 1; R_1 and R_2 oscillate between R_L and R_H in region 2; $R_1 = R_L$ and $R_2 = R_H$ in region 3. The output characteristics resemble the one of the CMOS inverters, except the transition region, *i.e.*, the second oscillatory region. A small decrease in the input voltage $V_{in} < 0.5V_{DD}$ leads to a high output $V_{out} > 0.5V_{DD}$, and, vice versa, the increase in the input voltage $V_{in} > 0.5V_{DD}$ leads to a low output $V_{out} < 0.5V_{DD}$.

Several CDW-based circuits can be cascaded. Figure 3(a) shows the two-input and one-output logic gates comprising three circuits similar to the one presented in Figure 2(a). The circuits are arranged in two stages. There are two circuits in stage one, and one circuit in stage 2. Two voltages, $V_{in}1$ and $V_{in}2$ are applied to the inputs of the first-stage circuits. The applying of the input voltages initiate the switching between the CDW states resulting in the change of the output voltages of the first stage circuits V_1 and V_2. Next, the outputs of the first stage circuits V_1 and V_2 are applied in parallel to the third circuit. In turn, the applying of V_1 and V_2 results in the change of the output voltage. Figures 3(b)-(d) present the results of numerical modeling showing the change of the output voltage in time. There are three curves of different color in each plot. The black and the blue curves correspond to V_1 and V_2, respectively. The red curve shows the resultant output voltage V_{out}. The voltages are normalized to V_{DD}. The time scale is shown in normalized units R_LC. The logic 0 and 1 correspond to the two voltage levels: $0.3V_{DD}$ and $0.7V_{DD}$, respectively. In the initial moment of time, $R_1 = R_H$ and $R_2 = R_L$ for all three circuits, and $V_{in}1 = V_{in}2 = 0.5V_{DD}$.

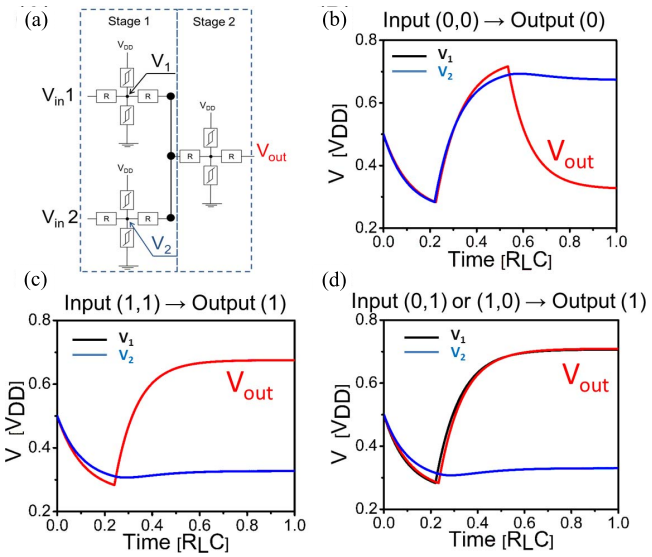

Fig. 3. (a) Schematic of the OR gate. (b)-(c) Results of numerical modeling showing the change of the output voltage in time in case (b): $V_{in}1 = V_{in}2 = 0.3V_{DD}$; (c) $V_{in}1 = V_{in}2 = 0.7V_{DD}$; (d) $V_{in}1 = 0.3V_{DD}$, $V_{in}2 = 0.3V_{DD}$. The time is shown in normalized units R_LC.

The decrease in the input voltages $V_{in}1 = V_{in}2 = 0.3V_{DD}$ leads to the increase of V_1 and V_2, and decrease in V_{out}, as shown in Figure 3(b). This function corresponds to the logic operation (0,0) → 0. The increase in the input voltages $V_{in}1 = V_{in}2 = 0.7V_{DD}$ leads to the decrease in V_1 and V_2, while V_{out} increases as shown in Figure 3(c). It corresponds to the logic operation (1,1) → 1. In the scenario where one or the other of the inputs has high voltage, *i.e.* $0.7V_{DD}$, the output voltage reaches its high value $V_{out} = 0.7V_{DD}$ as shown in Figure 3(d). It is equivalent to the logic operations (1,0) → 1 or (0,1) → 1. The whole circuit operates as the OR gate. It takes one oscillation to switch between the output states. Upon completion, the output voltage becomes constant. There are many possible combinations of the CDW-based circuits leading to different logic functionality. The combination of the inverter and the OR gate is sufficient for building all possible Boolean-type logic gates [12].

IV. Discussion

The described CDW-based logic circuits have certain unique features. They consist of only two-terminal CDW devices and regular resistors. Unlike conventional FETs, the switching in CDW-based devices is controlled by the source-drain voltage rather than by the gate voltage. No gate dielectric is used in the device structure. The metallic nature of the CDW channels, characterized by the high carrier concentration, and the absence of gate dielectric make the CDW circuits inherently immune to the radiation effects. Taking into account a very small change of the threshold voltage (less than 2%) in 1T-TaS_2 device under the X-ray ionization doses of up to 1-Mrad [7], one can expect similar high radiation immunity of the logic gates built on such devices. The effects of irradiation, if there are any, can be readily compensated by the change in the bias voltage V_{DD}, which enlarges the transition region II (see Figure 2(c)). In general, the output characteristics of the CDW-based circuits are defined by the set of parameters R_H, R_L, V_{HL}, V_{LH} and the bias voltage V_{DD}. The On/Off ratio is directly related to R_H/R_L, which, in turn, is a function of the carrier concentrations in the IC-CDW and NC-CDW states. The steepness of the switching depends on how close the phase transition voltages are V_{HL} and V_{LH} to the circuit stable points, *i.e.*, the voltage offset, ΔV. The shape of the noise margins is related to the $R/(R_H + R_L)$ ratio. The higher the resistance R, the flatter is V_{out}/V_{in} dependence in the Regions I and III (see Figure 2(c)).

The internal time delay of the CDW-based devices is defined by the nature of the phase transition. It has been suggested that the transitions between IC-CDW and NC-CDW phases in 1T-TaS_2 channel can be as fast as ∼1 THz [13]. The inter-device delay, determined by RC constant, can be minimized since the operation of the CDW logic gates does not involve charging and discharging of the gate capacitors. The area of the logic gates can be optimized by exploiting multi-input schemes similar to one shown in Figure 3(a). One can envision a design with multiple inputs to one CDW device, with the output controlled by the majority of inputs, *e.g.*, MAJ gate. The current through the pair of CDW devices connected in series is a direct analogy of the leakage current in CMOS. It can be minimized by increasing the ON/Off ratio, *e.g.*, by making R_H larger, or/and by decreasing V_{DD}.

In order to compare the CDW-based inverter with other proposed nanoelectronics devices, we adopted the methodology for beyond-CMOS devices benchmarking as described in [14]. Based on the available experimental data, we project the following device characteristics: $V_{HL} = 1$ V; $V_{LH} = 0.5$ V; $R_L = 1$ kΩ, $R_H = 1$ MΩ, area = 1 μm^2. The ultimate switching time is assumed to be 1 ps [13]. Based on these numbers, we can estimate the energy per operation to be 1 V × 1 mA × 1 ps = 1 fJ. The static power density is 1 V × 1 μA / 10^{-8} cm^2 = 100 W /cm^2. The possibility of using the multi-input CDW devices for MAJ gate construction gives a substantial advantage in constructing more sophisticated logic circuits. The estimates for the 32-bit CDW adder circuits give 10 μm^2 area, 50 ps delay time, 10 fJ energy per operation, and 200 Pops/s/cm^2 throughput. Most of these characteristics, particularly delay time and throughput, compare favorably with those of the complementary metal-oxide-semiconductor (CMOS) HP and LP, as well magnetic logic circuits such as nano-magnetic logic (NML) and spin torque transfer-domain wall (STT-DW)) [15]. The latter technologies are considered to be the most promising approaches among the radiation hard logic circuitries [16].

V. Conclusions

We proposed the design and simulated operation of the logic gates implemented with 2D CDW devices, which operate at room temperature. The building blocks of the logic gates have been fabricated and tested experimentally. The measured IV characteristics were used as inputs to the numerical models. The unique output characteristics of CDW devices allow for building logic gates without any transistors. Fast operation, scalability, and the possibility of building multi-input logic gates are the most appealing properties of the considered CDW devices. Owing to the radiation-hard nature of the "all metallic" CDW devices and absence of transistors the proposed circuits can be utilized in various harsh environments on earth or outer space.

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